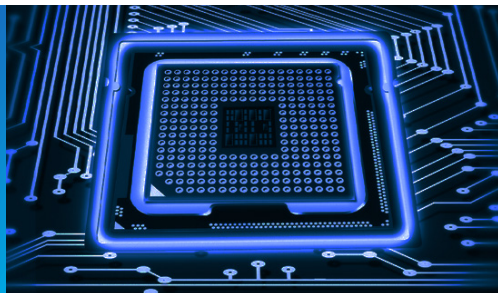
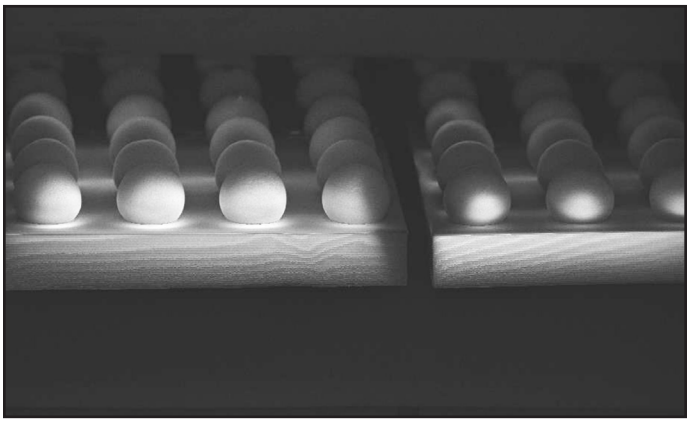
SPTS Etch and Deposition Processes for Advanced Packaging



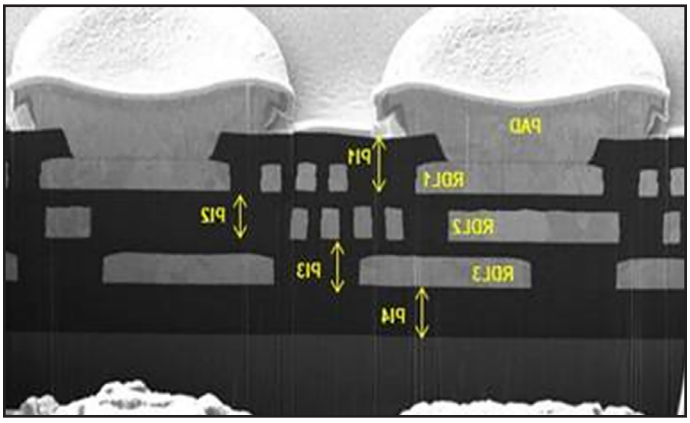
As the semiconductor industry looks beyond "Moore's Law", with dimensional scaling reaching its physical limits, new solutions are being developed to reduce chip size/height and lower production costs, while improving reliability, energy efficiency, device speed and multi-function integration.

KLA offers a range of plasma etch and deposition process technologies being used by leading semiconductor packaging companies for advanced packaging schemes - from High Density Fan-Out Wafer Level Packaging (HD-FOWLP) to the most advanced "3D" packages where two or more die, potentially for different functions, are stacked and connected in the vertical direction with through-silicon vias (TSV) filled with metal.

Leveraging our decades of expertise in deep silicon etching of MEMS and TSVs, KLA also offers the most advanced plasma dicing solutions for dicing before grind (DBG) or dicing after grind (DAG) of wafers up to 300mm in diameter, with optional overhead transport.



Plasma-diced bumped die on tape

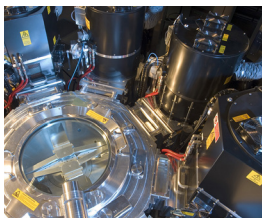


PVD-deposited re-distribution layers (RDL) in FOWLP structure

PROCESS MODULES

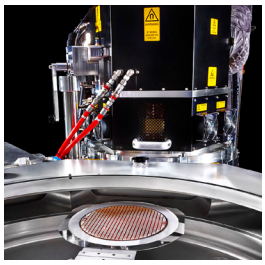
SPTS Omega® DSi-v / Rapier

Established high rate silicon etch modules with unique end-point solutions for TSV etch and wafer thinning.



SPTS Mosaic® Plasma Dicing

Low damage alternative to mechanical saw or laser dicing, for more die, cleaner die, and stronger die.



SPTS Delta™ PECVD

Deposition of stress-controlled SiO_x and SiN layers with unparalleled uniformity and deposition temperatures <250°C.

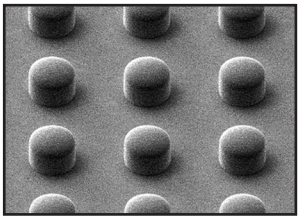
SPTS Sigma® PVD

High productivity metal layer deposition, with excellent film uniformity, for UBM/RDL and TSV barrier/seed layers.

PLASMA ETCH PROCESSES

Silicon Etching

The SPTS Omega® range of plasma etch systems includes the Rapier™ process module for high rate silicon etching in advanced packaging applications. Vertical or tapered, high aspect ratio via holes or slots can be created through silicon wafers or interposers which, once filled with conducting metals such as copper, form interconnects between different layers in the 2.5D/3D-IC package.



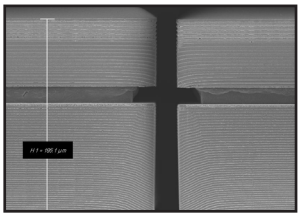
Blanket silicon on the back-side of a wafer reveals the base tips of the TSVs

Blanket via reveal etching is required to expose the Cu-filled vias from the backside of the wafer, prior to connection. The Rapier™ XE process module combines recipe-tuneable uniformity with an etch rate that is typically 2-4 times faster than competing systems for a blanket silicon etch. The same process can be used for extreme wafer thinning down to 5µm or even 0.5µm using an etch stop layer.

KLA offers unique, patent-protected end-point solutions for TSV etching, via reveal and extreme thinning processes which enable optimal throughput and yields in high volume production.

Plasma Dicing

The SPTS Mosaic™ plasma dicing systems offer an alternative to mechanical saw or laser technologies, for singulation of die from a silicon wafer (up to 300mm, on frames).



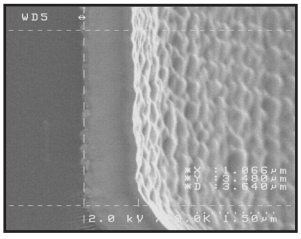
Bonded wafer singulated by plasma dicing

This solution offers a low damage, dry chemical process which increases die strength and avoids particulate contamination. These benefits are especially important when the wafers are thin or contain fragile low k films and for die to wafer bonding.

Being a parallel process, plasma dicing can offer significant throughput, yield and cost advantages when dicing small die and/or thin wafers. Dicing lanes can be much narrower than the equivalent lanes for saws or lasers, allowing more die per wafer. Additionally the dicing lanes need not be straight lines, offering more freedom for die shape/size and optimized wafer layouts.

DEPOSITION PROCESSES

Low Temperature Plasma Enhanced Chemical Vapor Deposition (PECVD)



PECVD oxide barrier near the base of a TSV

For advanced packaging applications, the SPTS Delta™ PECVD system offers low temperature dielectric deposition processes compatible with 300mm bonded substrates and mold. Applications include via-last TSV liner, via-reveal passivation and hybrid bonding.

Delta™ PECVD produces high quality, production qualified SiO and SiN films at deposition temperatures as low as 110°C. SiN – SiO stacks can be deposited in the same PECVD chamber with unrivalled electrical performance and stability over time. Film and stack stress can be tuned across a wide range and optimised chamber hardware enables the lowest within-wafer stress range available from any PECVD system. Where required, single-wafer and multi-wafer degas options are available to heat outgassing substrates and improve deposited film quality. Optimized SiO, TEOS SiO and other advanced dielectric films are available for fusion bonding applications.

Physical Vapor Deposition (PVD) for Metal Deposition

The SPTS Sigma® PVD systems are used to deposit metals such as Au, Al, Ti, TiW and Cu on Si or mold wafers. The adoption of organic passivation and new substrate materials for advanced packaging technologies present technical challenges for UBM/RDL. Using novel degas and pre-clean technology, the Sigma® fxP produces consistently low Rc values whilst delivering a 2x throughput advantage over other PVD systems. In 2.5D and 3D-IC applications, the SPTS Advanced Hi-Fill™ ionized PVD source delivers world-class Cu barrier/seed coverage in high aspect ratio TSVs.

KLA SUPPORT
Maintaining system productivity is an integral part of KLA's yield optimization solution. Efforts in this area include system maintenance, global supply chain management, cost reduction and obsolescence mitigation, system relocation, performance and productivity enhancements, and certified tool resale.

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