KLA✛

PWG5™

Wafer Geometry and Nanotopography Metrology System

The PWG5™ patterned wafer geometry metrology platform produces comprehensive wafer warp, bow, dual-sided nanotopography, high-resolution distortion, in-plane displacement and stress measurements for IC manufacturers. Built on the industry-standard WaferSight™ platform, PWG5 incorporates innovative hardware technology and unique features that support patterned wafer applications with repeatable high precision measurements. These measurements support the most extreme wafer warp requirements for R&D and the most cost-effective inline monitoring applications for high volume manufacturing. PWG5 is a single-tool solution for measuring stress-induced wafer shape, wafer shape-induced pattern overlay errors, wafer front and backside nanotopography, and wafer thickness variations. PWG5 enables faster process ramps and higher yields, providing overlay control through process monitoring and data feed forward, lithography focus window control, and inline monitoring for processes such as thin films, etch, CMP and RTP.

As the latest-generation PWG system, the PWG5 enables wafer geometry control for both patterned and unpatterned wafers for ≥96 layer 3D NAND devices and ≤1Xnm logic and DRAM design nodes. Compared to previous generation PWG systems, the PWG5 incorporates new hardware technologies and algorithms that enable enhanced capability, including:

- Industry-best warp dynamic range, up to 1000μm, for inline monitoring and control of wafer warp and stress resulting from advanced 3D NAND deposition processes

- Spatial resolution of 40μm and high data density for intra-die stress monitoring to counter process-induced overlay variations

- High throughput for inline measurements that drive process corrections during high volume manufacturing

PWG5 Measurement Capabilities

With industry-unique vertical wafer hold, PWG5 metrology systems provide full wafer, simultaneous measurement of front and back wafer surfaces without gravitational distortion effects. A single measurement produces the following wafer metrics:

- Warp and bow
- In-plane displacement
- Stress-induced local curvature
- Wafer thickness and flatness variation
- Front and back surface Nanotopography (NT)
- Wafer edge roll-off (ERO)

Simultaneous measurements of front and back side of wafer

**Industry-unique vertical wafer hold minimizes gravitational distortion**
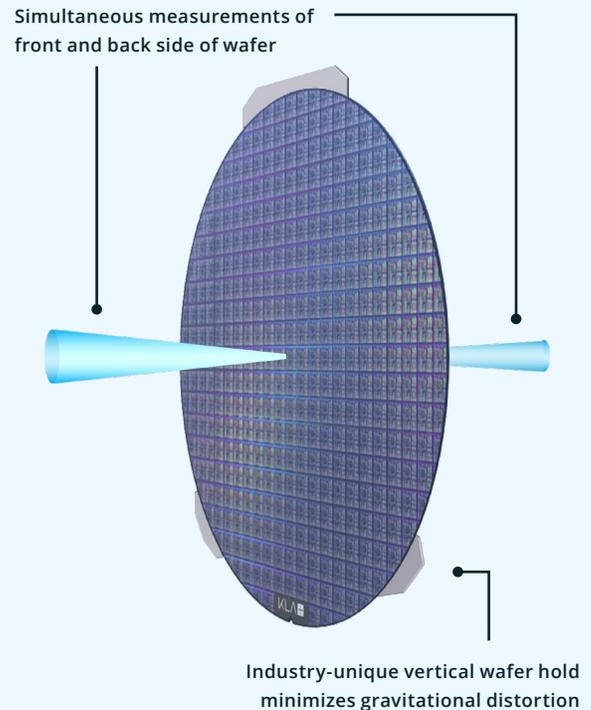
Many IC process steps can cause wafer warp, bow, distortion, stress and nanotopography variations that directly impact pattern integrity and final device performance. The PWG5 metrology system identifies and monitors these issues inline, helping IC manufacturers drive improvements in their processes.

- **In-plane displacement.** Process induced shape changes cause distortion-inducing in-plane displacement within the wafer when it is chucked on the lithography scanner. When not corrected for, in-plane displacement can cause excessive overlay residuals.
- **Edge roll-off.** Deviations in a wafer's edge roll-off (ERO) can create defocus defects near the wafer's edge, reducing the ability to print yielding edge die.
- **Nanotopography.** The uniformity of material removal during CMP can be influenced by nanotopography.
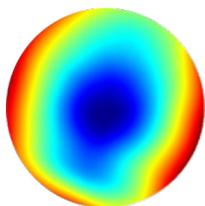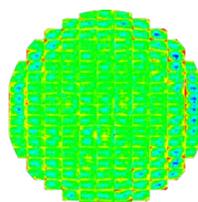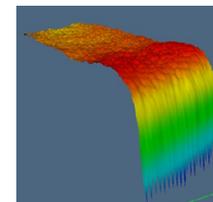

Shape Change
CVD, PVD, Anneal, Etch, CMP
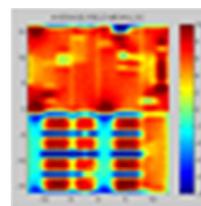
Intra-die Stress
CVD, PVD, Anneal, Etch, CMP
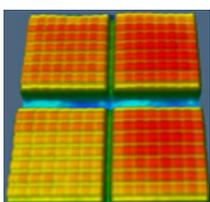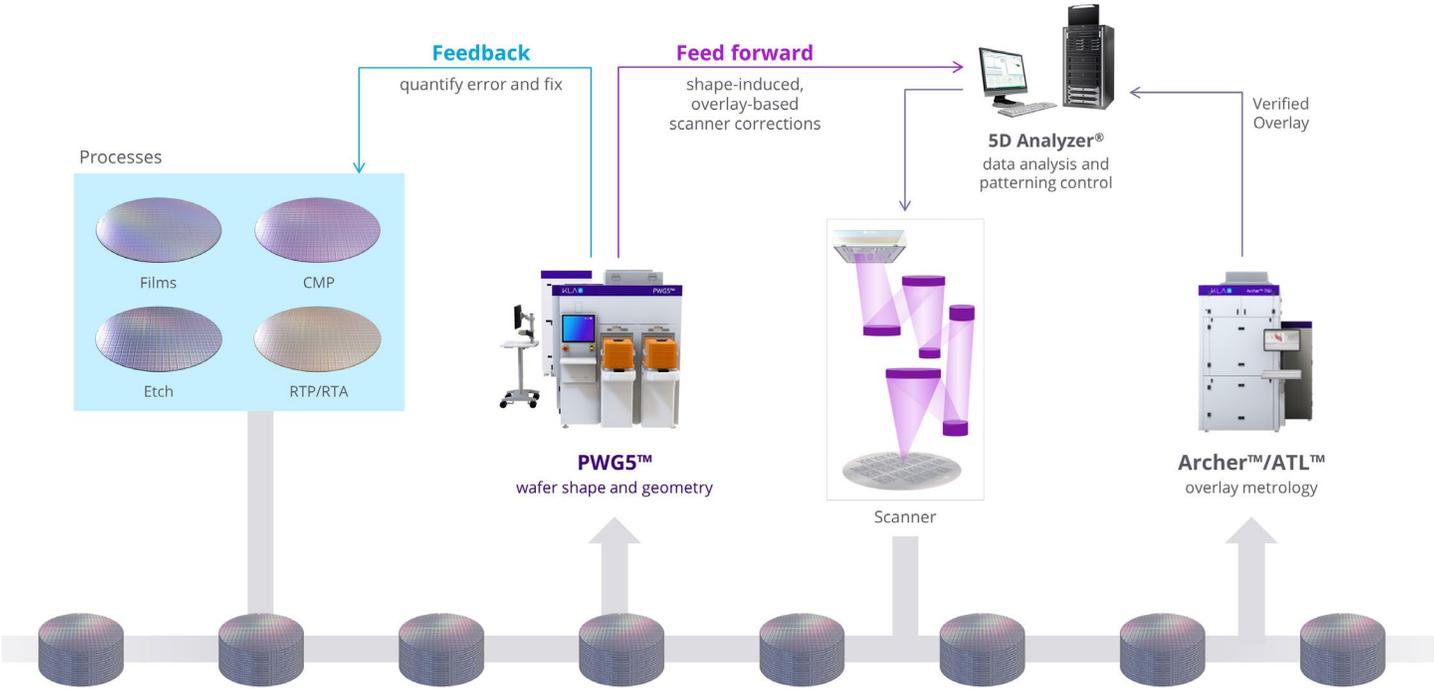

Local Topography
CMP

Flatness
CVD, PVD, CMP

Edge
CVD, PVD, CMP

PWG5 is part of a comprehensive portfolio of metrology and data analytic products that help IC manufacturers maintain tight control of their processes for improved device performance and yield. The PWG5 metrology system outputs measurement results to the fab's host as well as to KLA's 5D Analyzer® advanced data analysis and patterning control software. Using this information, lithography engineers can understand whether shape-induced overlay can be compensated for by adding additional overlay corrections, including corrections to existing APC (Advanced Process Control). Shape overlay corrections output from PWG5 and 5D Analyzer can be combined with non-shape overlay corrections to generate a final, comprehensive correction file for scanner exposure. With proper PWG5 and 5D Analyzer infrastructure setup, this workflow can be done manually by engineers or automatically by the host.

Feedback
quantify error and fix

Feed forward
shape-induced,
overlay-based
scanner corrections

5D Analyzer®
data analysis and
patterning control

Verified
Overlay

Processes

Films

CMP

Etch

RTP/RTA

PWG5™
wafer shape and geometry

Scanner

Archer™/ATL™
overlay metrology

KLA+

PWG5 Applications

The PWG5 metrology system can be used to qualify, monitor and control processes in both feedback and feed forward modes. Proven metrics enable faster root cause determination, helping fabs reduce process development time. In addition, the PWG5 offers multiple applications that help expand overlay and focus process windows for ≥96 layer 3D NAND device fabrication, and advanced logic and DRAM design nodes.

- Correction of wafer shape induced overlay error for reduction of wafer-to-wafer and lot-to-lot variability and improvement of final ADI on-product overlay

- Intra-die stress signature detection for cost effective and accurate intra-die overlay prediction and monitoring

- Identification of sources of higher order shape components of lithography overlay residuals that cannot be addressed through scanner corrections; by measuring the wafer's back side, PWG5 eliminates pattern effects from front side

- Optimization and inline monitoring of film deposition and RTP processes for control of wafer shape changes

- Chamber matching of film deposition tools, such as CVD and PVD

- Inline monitoring of local wafer stresses due to film deposition processes for vertically integrated devices, such as 3D NAND

- Optimization of lithography reticles based on intra-field overlay and stress variations

- Inline monitoring of CMP processes for wafer flatness and/or nanotopography for reduction of scanner defocus at downstream lithography operations

- Qualification and inline monitoring of ERO characteristics of bevel etch processes that impact scanner depth of focus (DOF) budget at the wafer's edge

- Monitoring of thickness variations on thick, opaque hard mask layers

- Extendibility to wafer-to-wafer bonding measurements for advanced wafer-level packaging applications