Application of Inline Defect Part Average Testing (I-PAT™) to Reduce Latent Reliability Defect Escapes

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AEC Program Update
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Outline

1. Introduction and Problem Statement
2. I-PAT Description
3. I-PAT Implementation Examples
4. Next Steps

KLA: Quality Partner for the ICs that Power the Future of Automotive

Automotive Commitment and Expertise

Ann Arbor, MI

- R&D Center
- Automotive and AI

Commentary

- Process Watch
- Semiconductor Engineering
- ECN, Elektronik, …

Workshops

- Auto fabs
- Tier 1s
- OEMS

http://www.kla.com/automotive

Quality Control Solutions for Automotive ICs

Continuous Improvement

- Surfscan® Series

Zero Defect Screening

- 8 Series
- Certified and Relaunched

Advanced Design Node

- 39xx and 29xx Series
- eDR7xxx™ Series

Packaged IC Quality

- ICOS™ Series

Power Device Reliability

- Candela® CS920

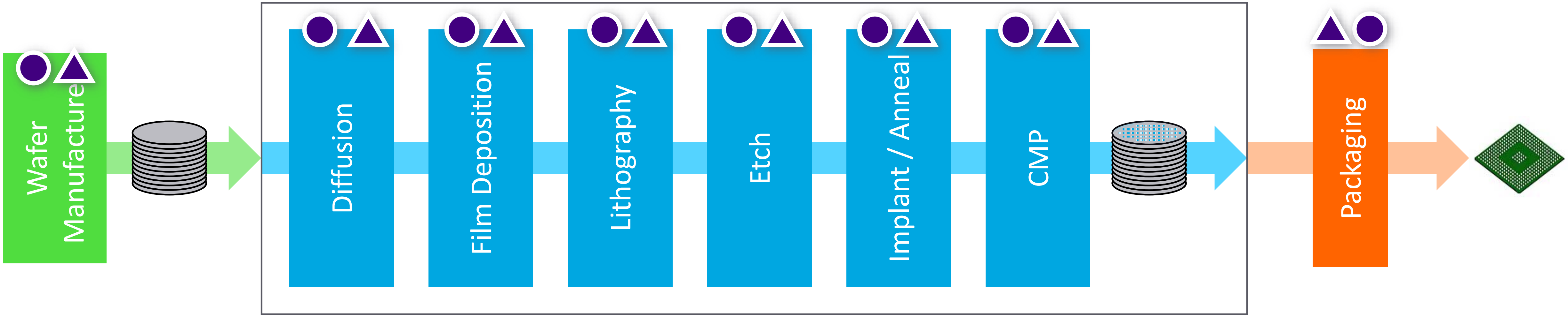
Inline Inspection and Metrology Data

Collected Across the Entire Semiconductor Process

● **Inline Defect Inspection**

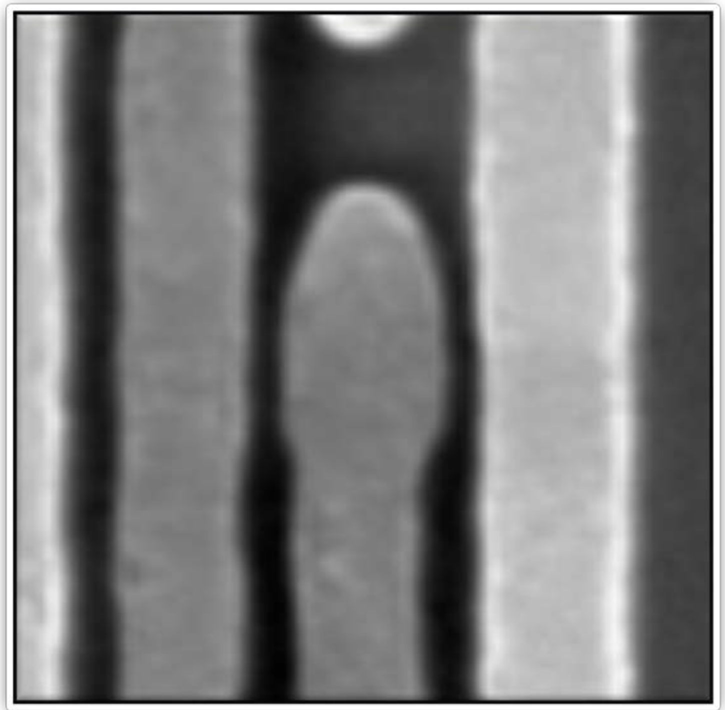
▲ **Inline Metrology**

- 500 – 1000 process steps
- 50 – 300 defect inspection steps*
- 50 – 100 metrology measurements*

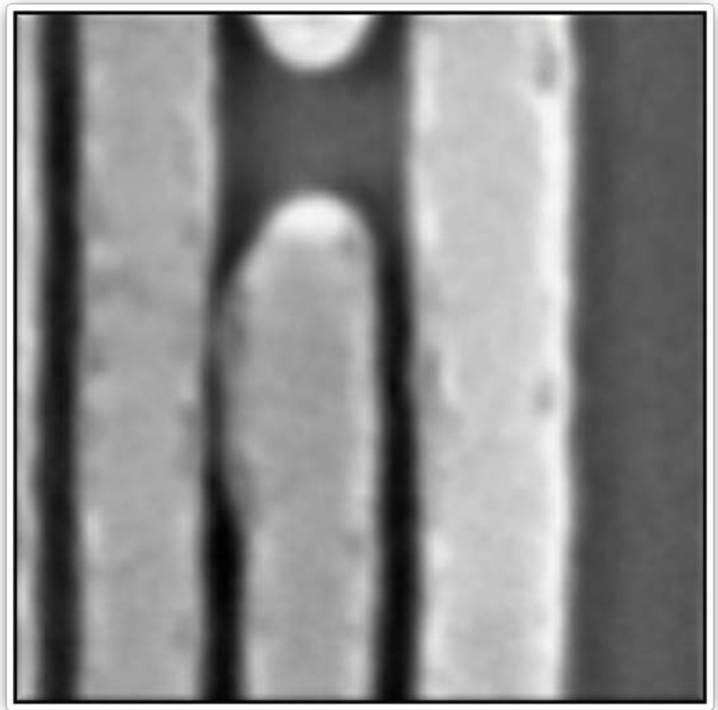


*usually applied on a sampling basis

The Automotive Defect Problem: Latent Reliability Failures



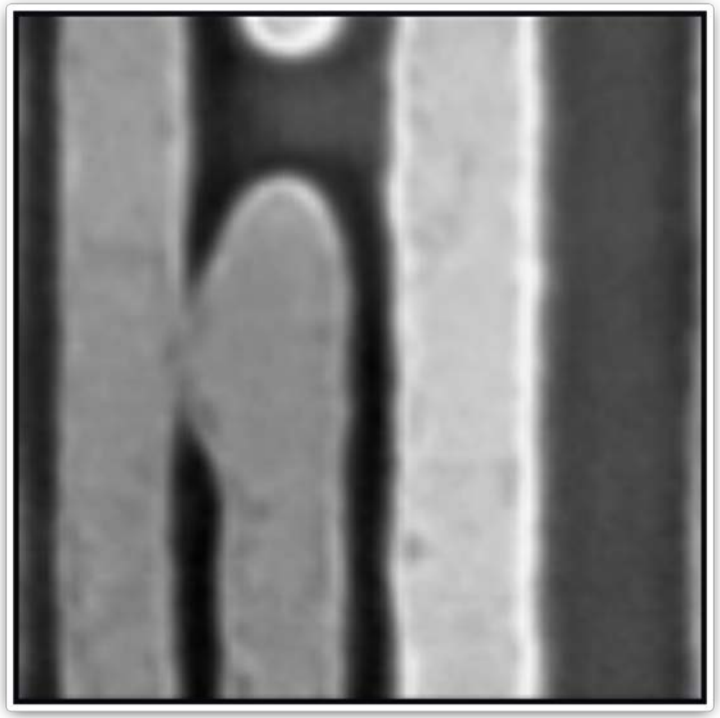
Good Die



Low Reliability

Passes test…

sometimes fails in the field

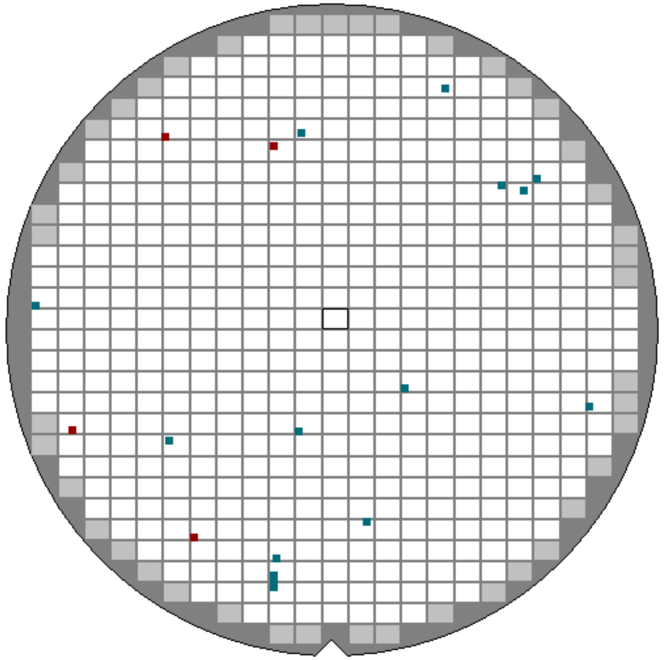


Bad Die

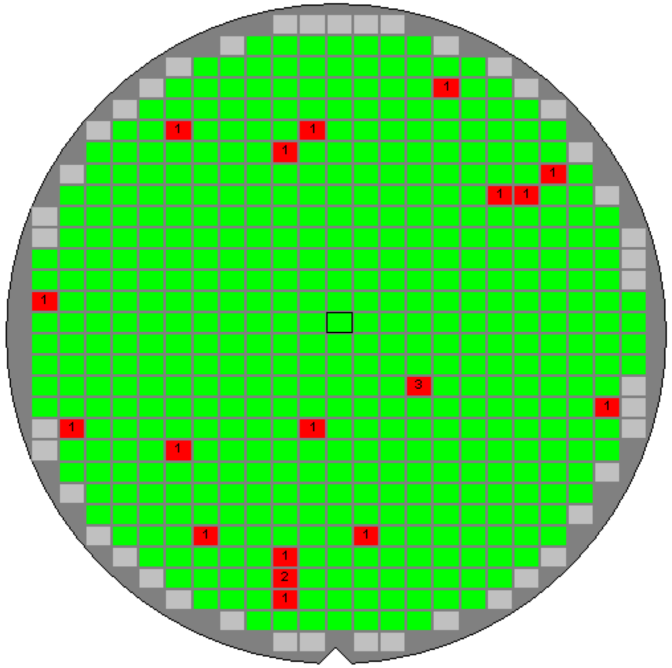
Fails test

Die-Level Defect Screening

Inline Defect Wafer Map from Screening Layer



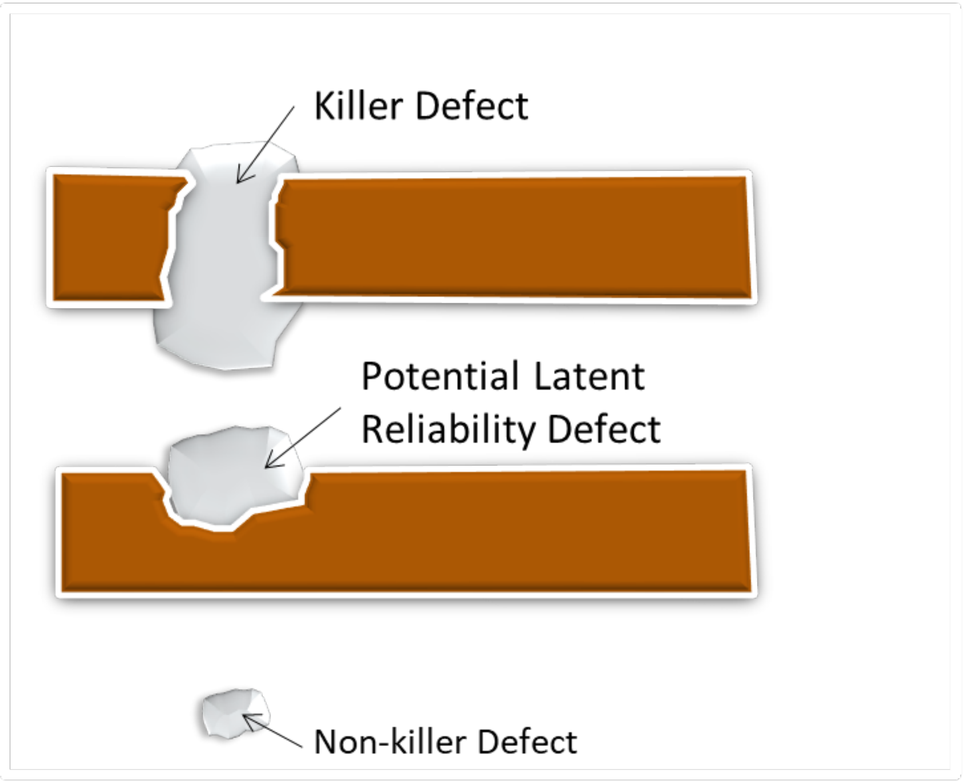
Inking Map



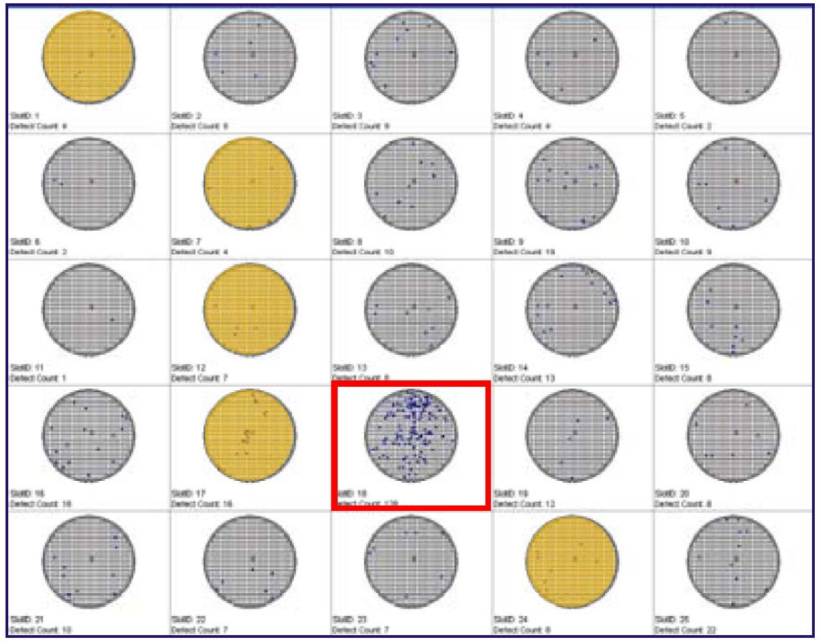
1. 100% of wafers are scanned
2. Results used to downgrade or scrap

Why Do Die-Level Screening?

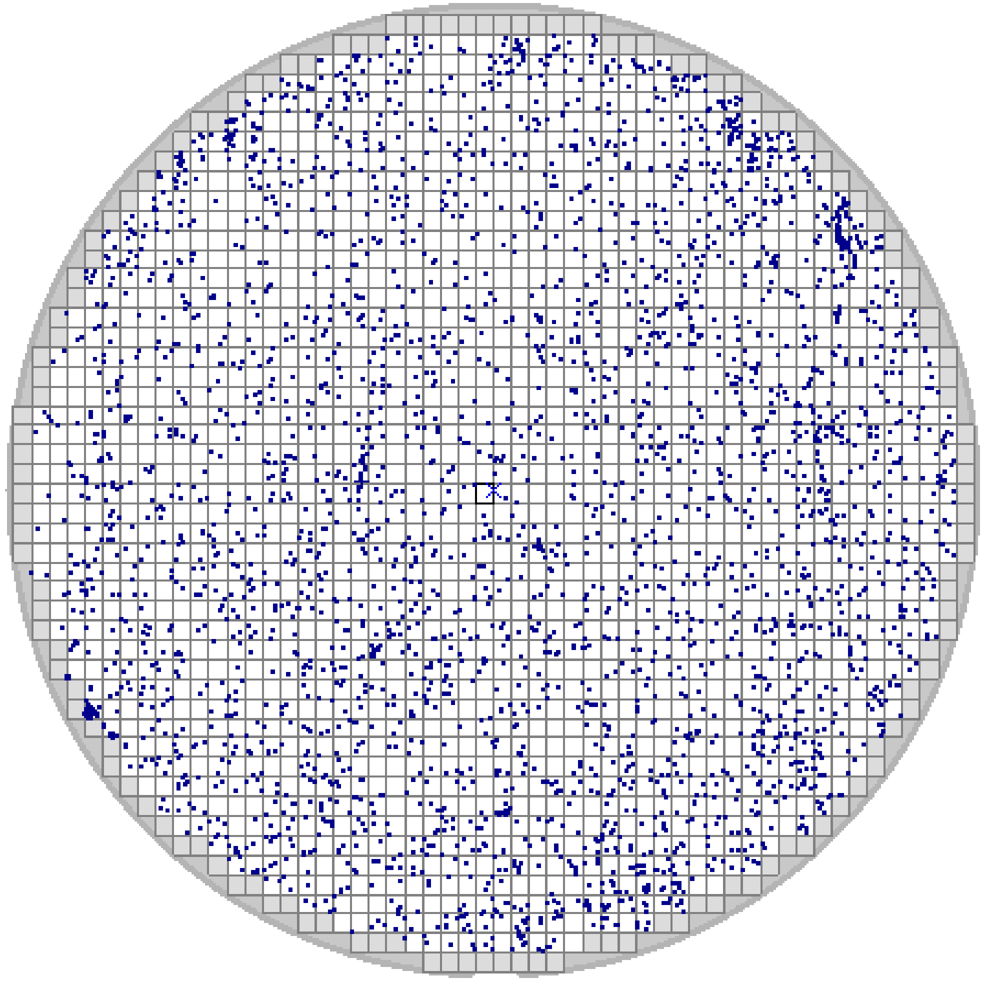
On-wafer random defectivity
is the main culprit for 0km
and field failures



Single wafer excursions
are common and slip through
most sampling schemes



Screening Challenge: Overkill



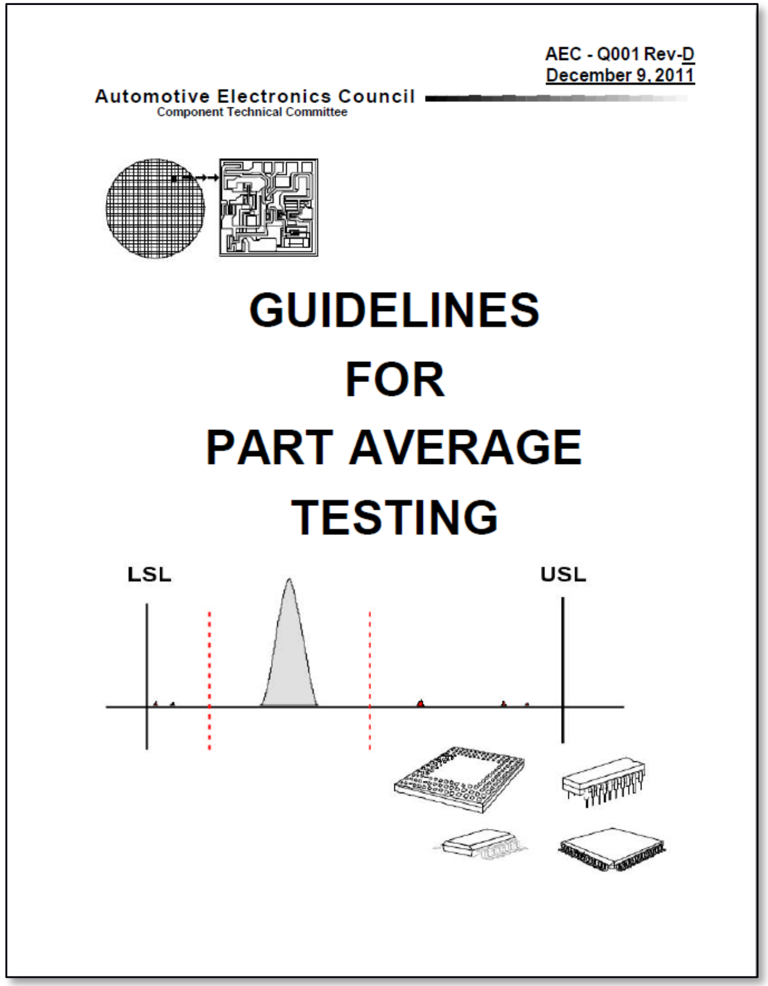
Which defects really matter?

- Typically 100s – 1000s of defects
- No time for review and classification

I-PAT Approach:

- Weight defectivity by relevance
- Apply outlier detection methods to reduce overkill

Part Average Testing



AEC - Q001 Rev-D
December 9, 2011

Automotive Electronics Council
Component Technical Committee

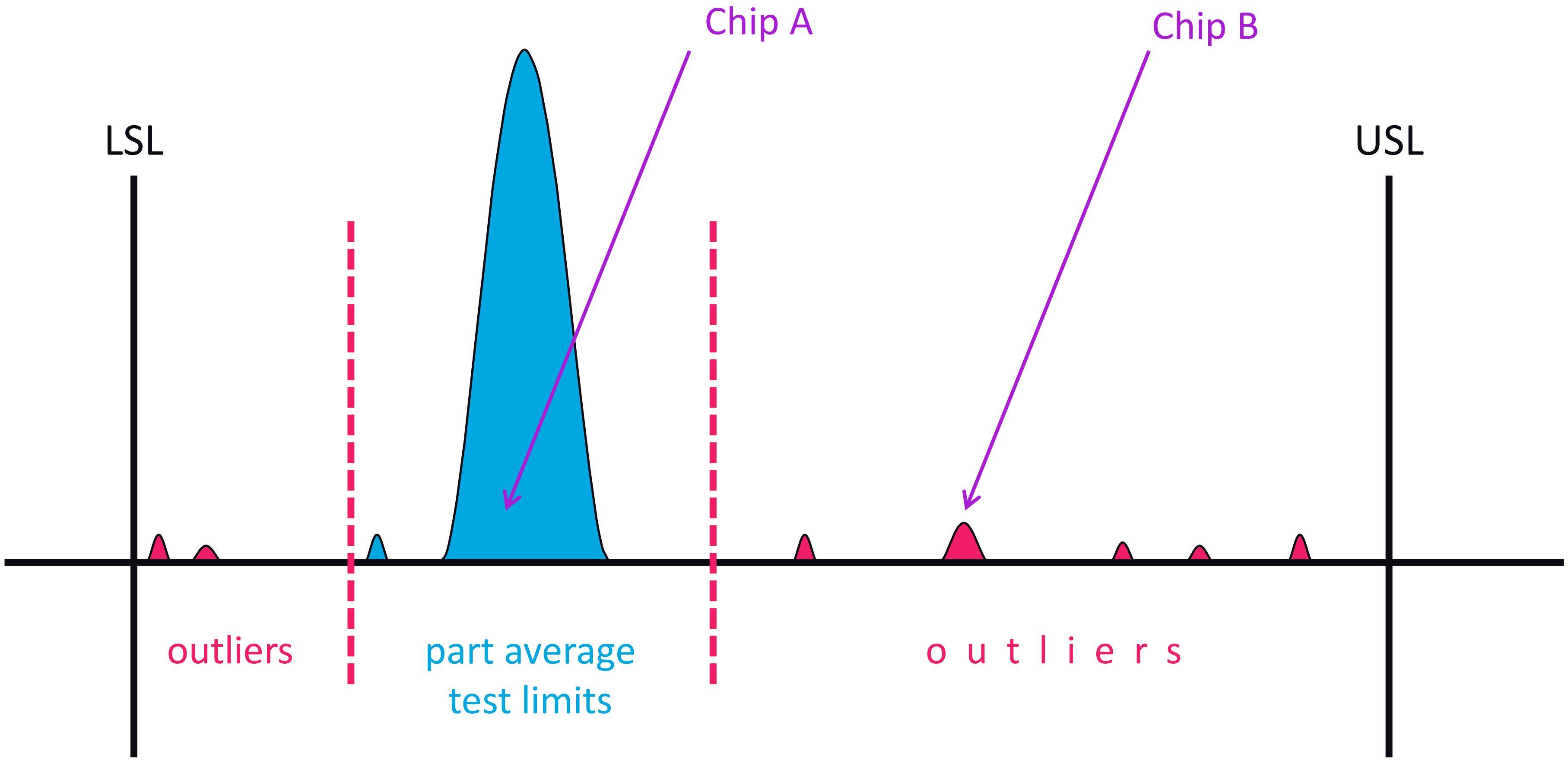
GUIDELINES
FOR
PART AVERAGE
TESTING

- Statistical screening technique
- Introduced by AEC in 1997

Assumes die outside of the normal distribution (but inside the spec limit) have a higher chance of reliability failures.

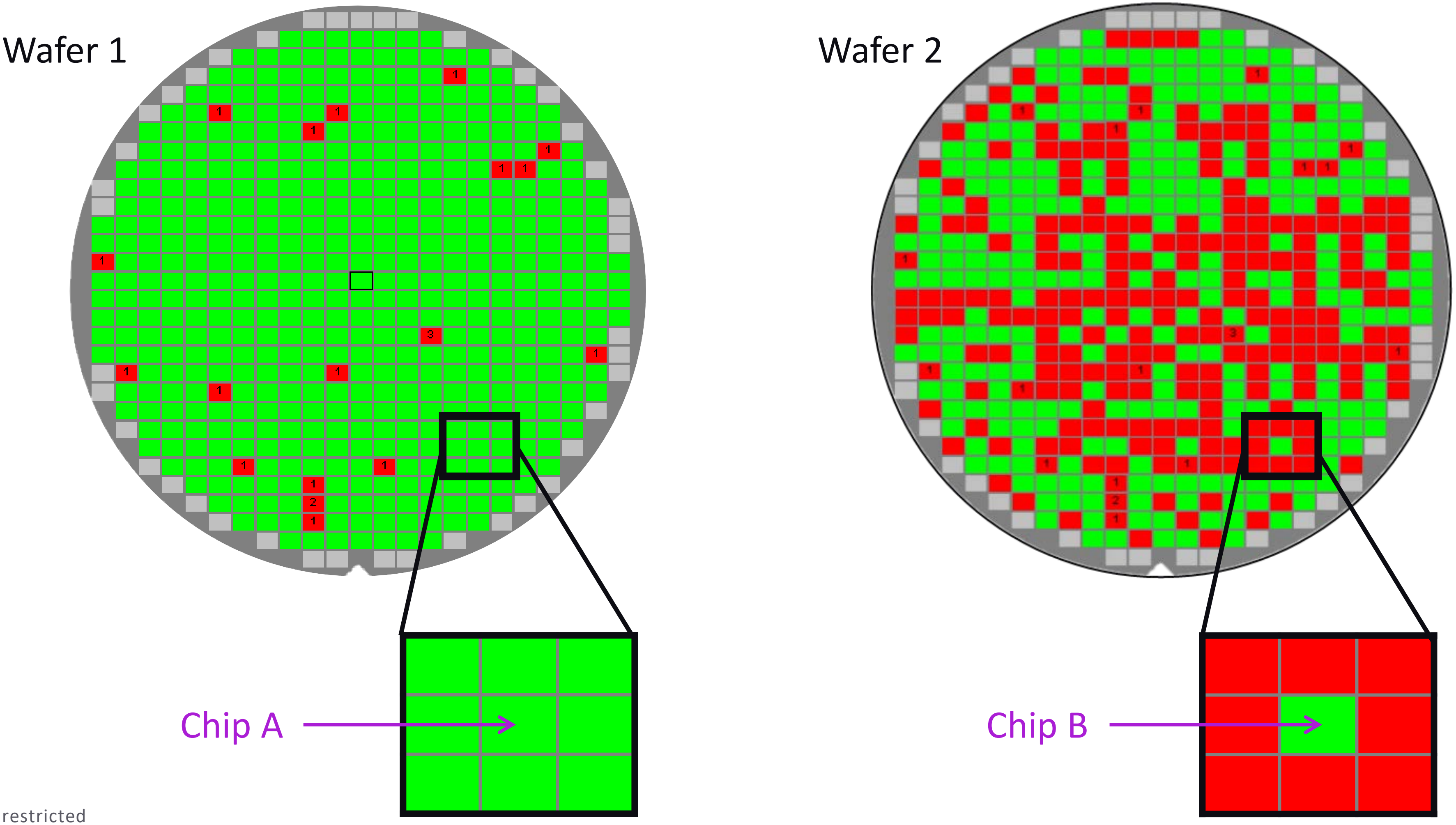
Parametric Part Average Testing (P-PAT)

Is there a **statistical** difference in chip reliability between Chip A and B?



Geometric Part Average Testing (G-PAT)

Is there a **statistical** difference in chip reliability between Chip A and B?



Inline Part Average Testing (I-PAT)

Is there a **statistical** difference in chip reliability between Chip A and B?

Inspection Layer 1

Inspection Layer 2

Inspection Layer 3

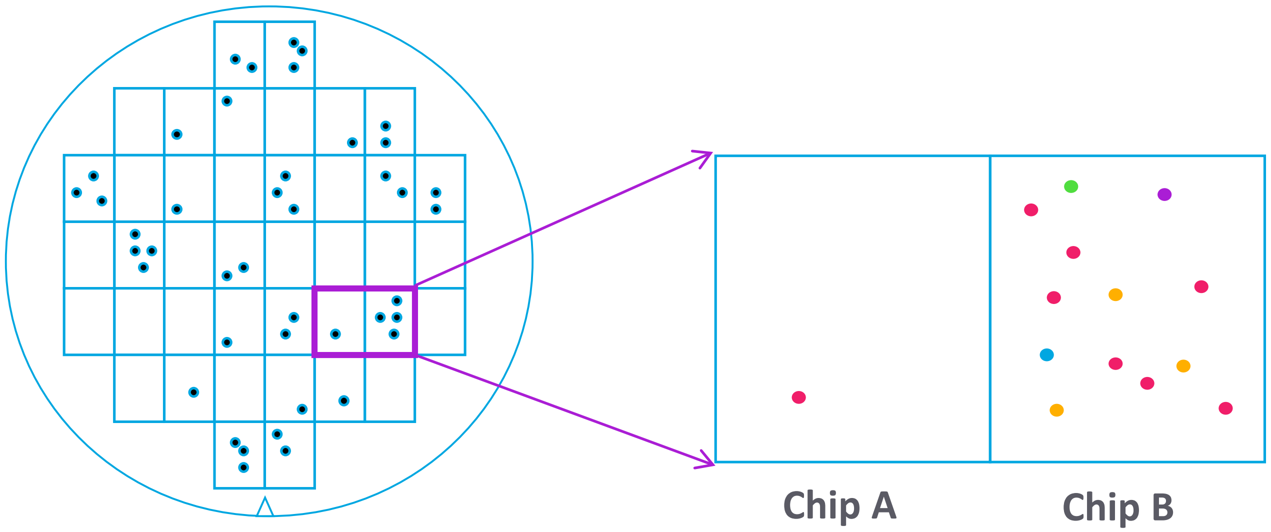
Inspection Layer 4

Inspection Layer 5

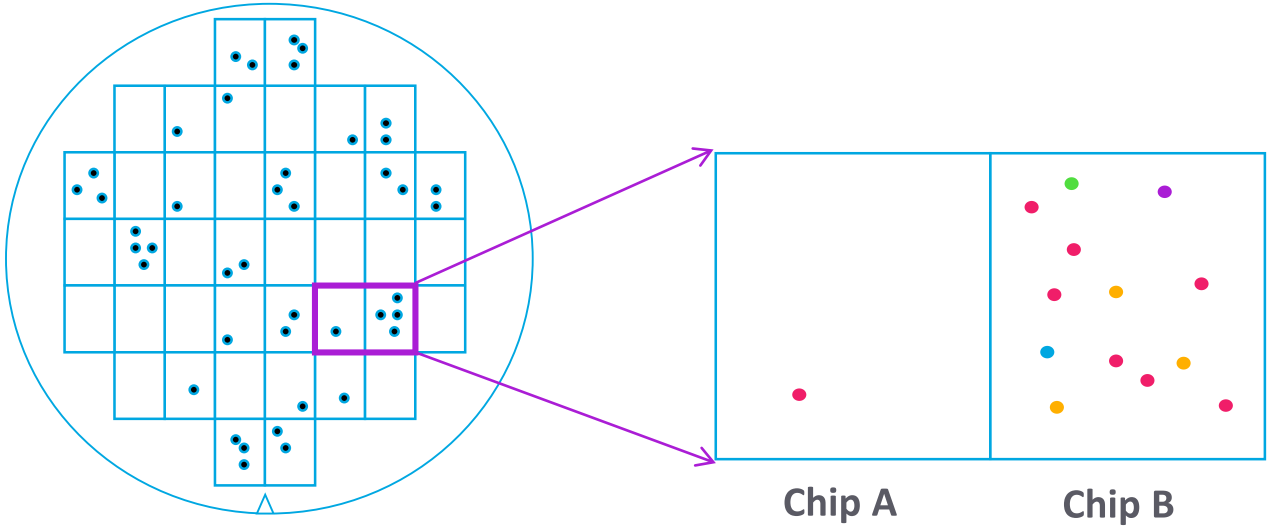
.
.
.

Inspection Layer N

Stacked-defect die map created by adding together the defects from multiple inline inspection steps



Simple I-PAT Implementation



$$P\ (LRD)_i = N_i\, m$$

The probability of die i having a latent reliability defect = The total number of defects in die i. X The ratio of latent reliability defects to total defectivity $(0 < m << 1)$

Chip B has a 15x higher statistical probability of a latent reliability failure than Chip A

Predicated on the observation that the probability distribution of latent defectivity roughly follows the distribution in total defectivity

No DOE required. Plug and play

Simple I-PAT Illustration

4 nominal layers
1 layers with
small signature

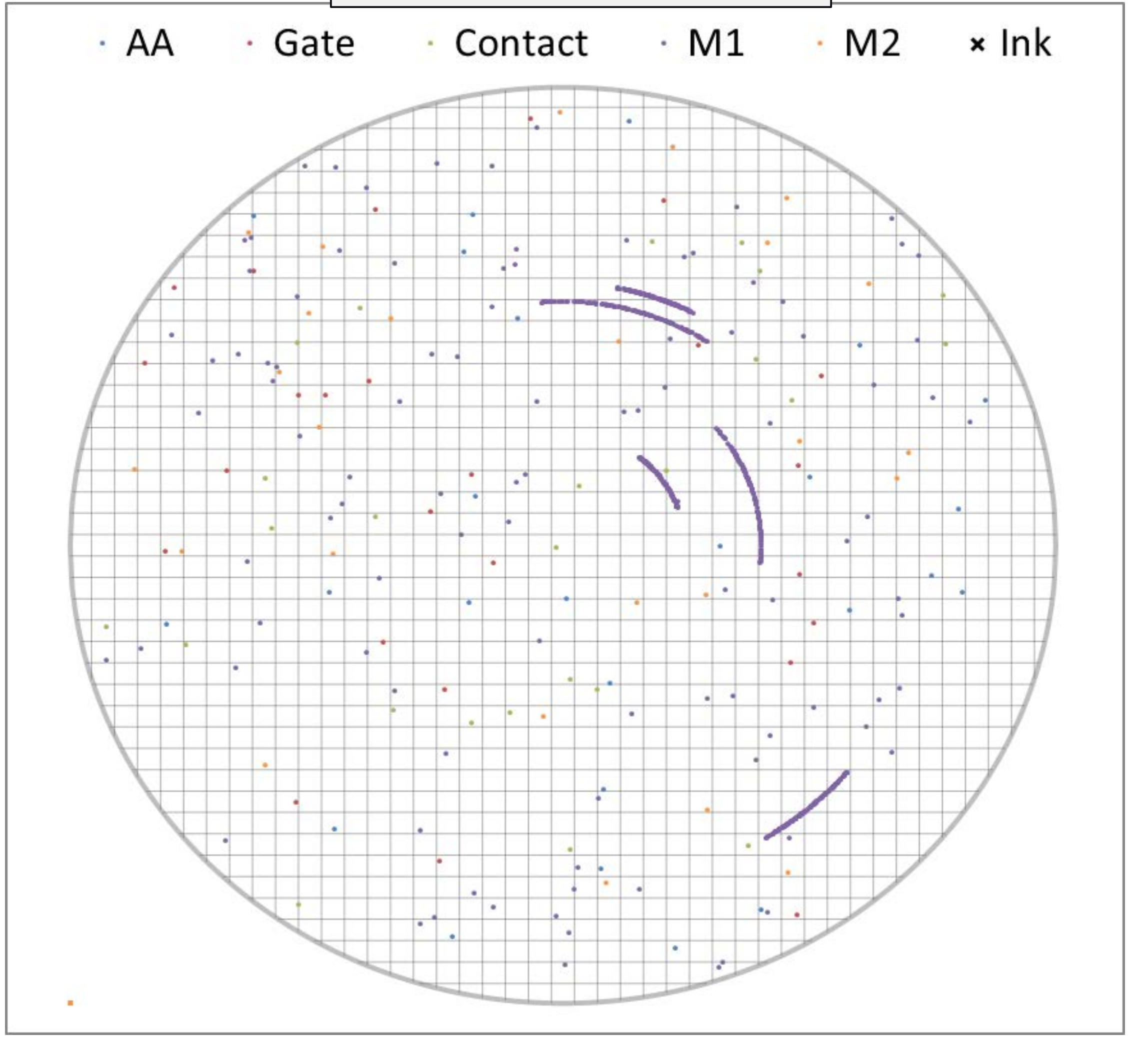
Defects	AA	Gate	Contact	M1	M2
Profile	Flat	Flat	Flat	Scratches	Flat
Defects	25	25	25	800	25

Global	
Die Size (mm)	7.00
Die Area (mm^2)	49.00
Die / Waf (est)	1354
Failures	10

Ink out die worse than # 1 (> 47)

	Failed	Inked	Inked %	Found	Found %
AA	1				
Gate	0				
Contact	0				
M1	9				
M2	0				
Stacked	10				
Total	**10**	**0**	**0.0%**		

Stacked defect wafer map



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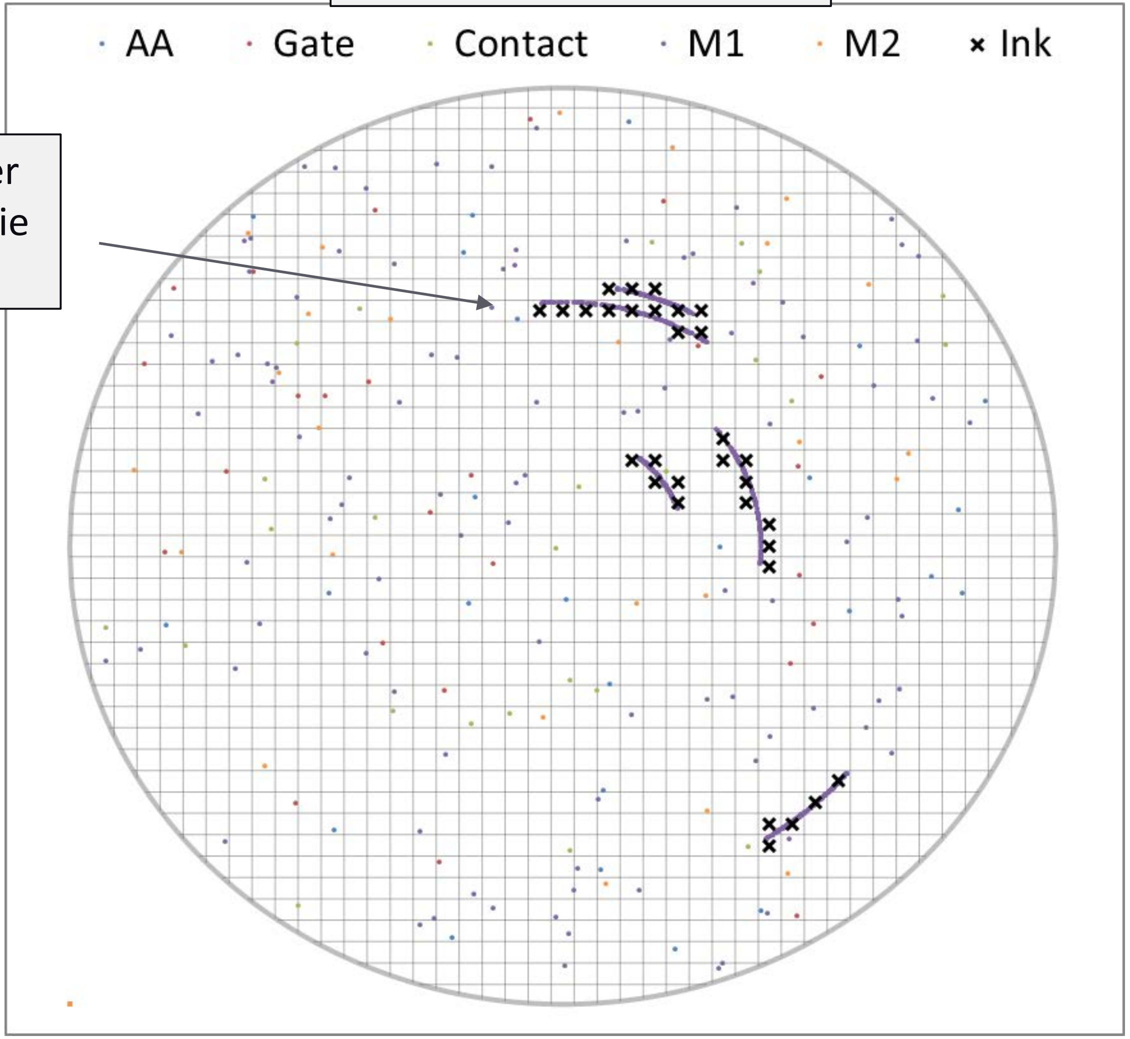
I-PAT identifies the outlier die based on # defects/die and inks them out (X).

Ink out die worse than # 32 (> 3)

	Failed	Inked	Inked %	Found	Found %
AA	1				
Gate	0				
Contact	0				
M1	9				
M2	0				
Stacked	10				
Total	**10**	**31**	**2.3%**		

Stacked defect wafer map



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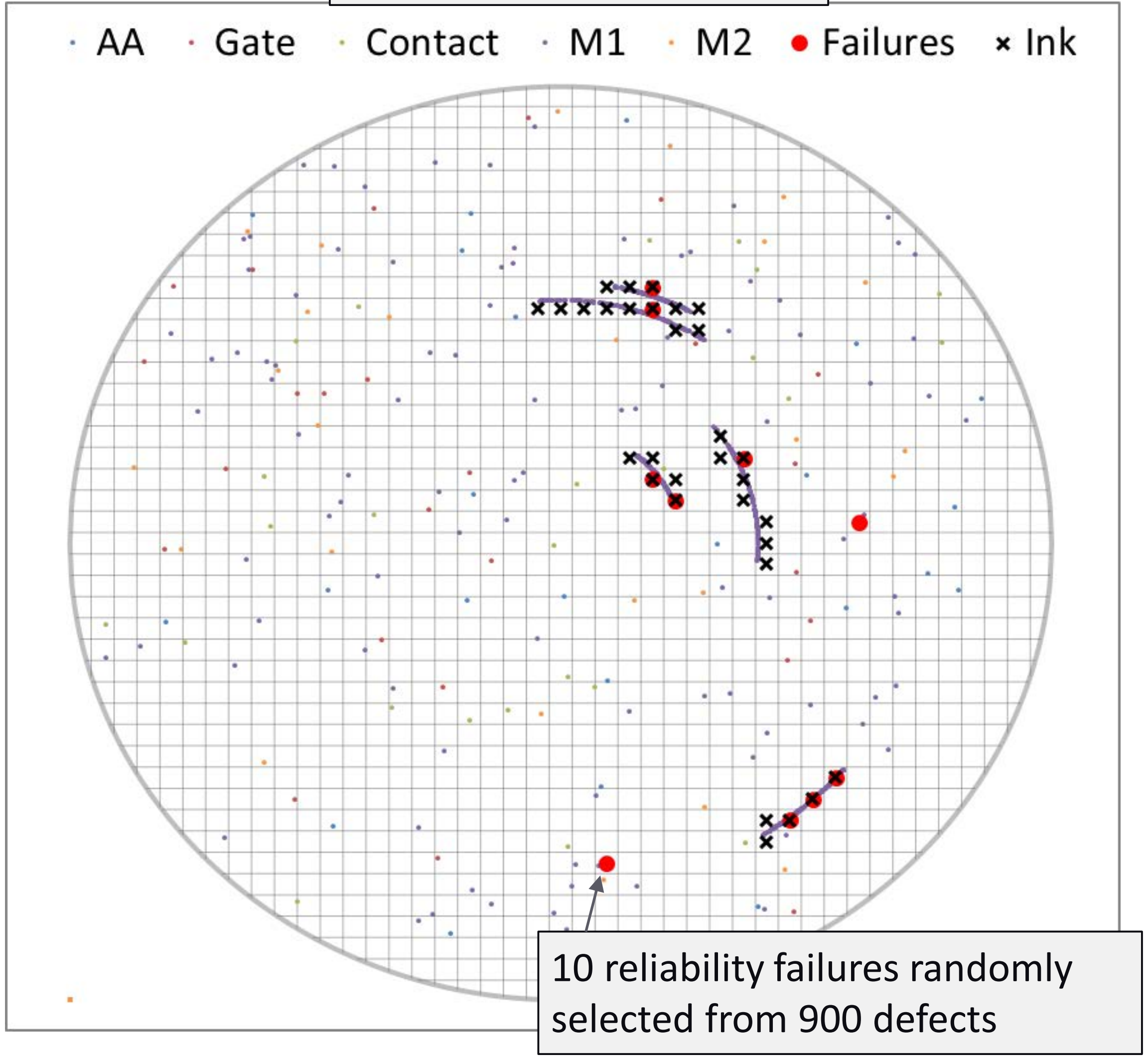
Contact	0				
M1	9				
M2	0				
Stacked	10				
Total	**10**	**31**	**2.3%**	**8**	**80.0%**

Stacked defect wafer map



10 reliability failures randomly selected from 900 defects

Simple I-PAT Illustration

4 nominal layers
1 layers with
small signature

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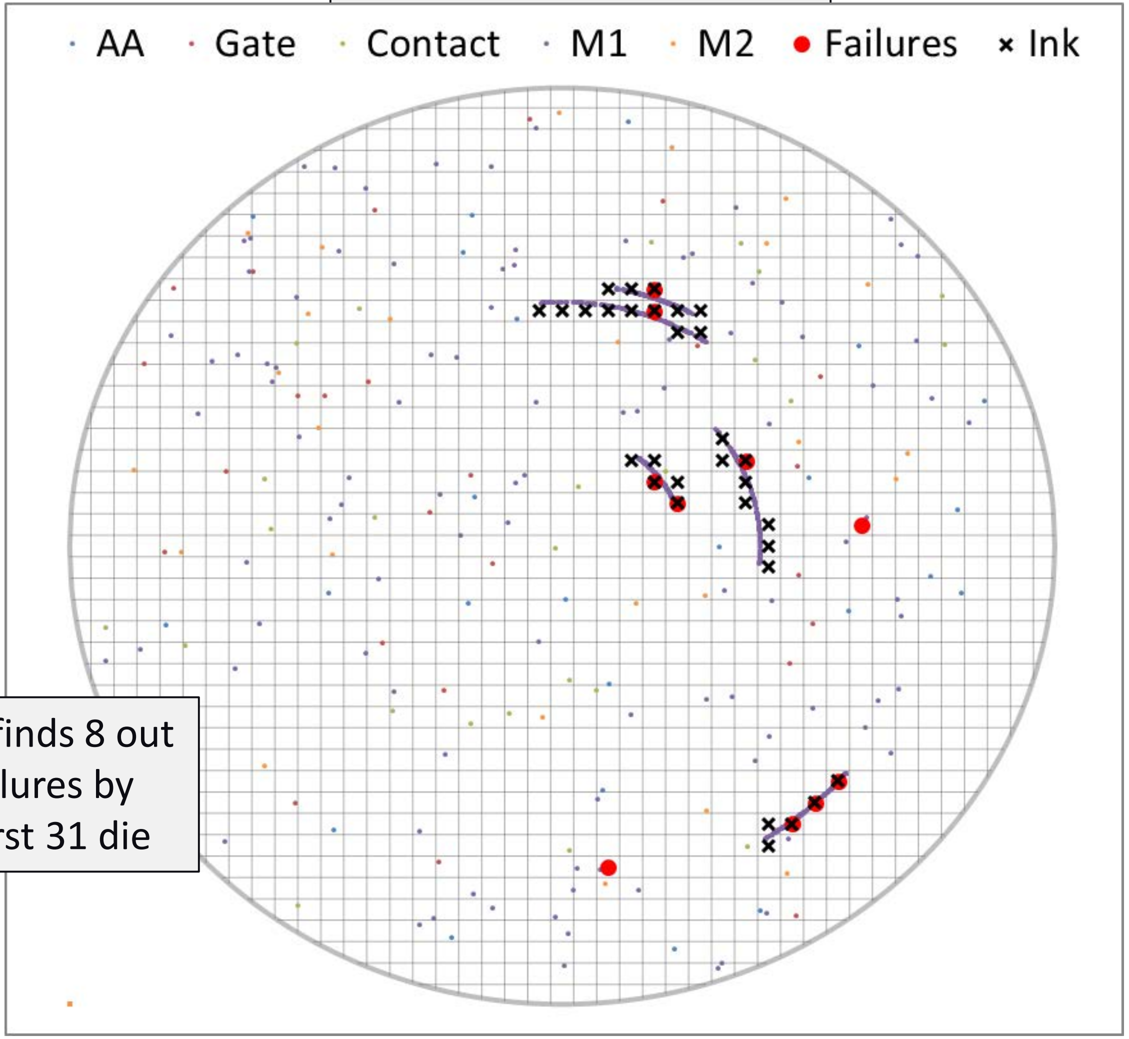
Stacked defect wafer map



Simple I-PAT algo finds 8 out of 10 reliability failures by inking out the worst 31 die

Smart I-PAT

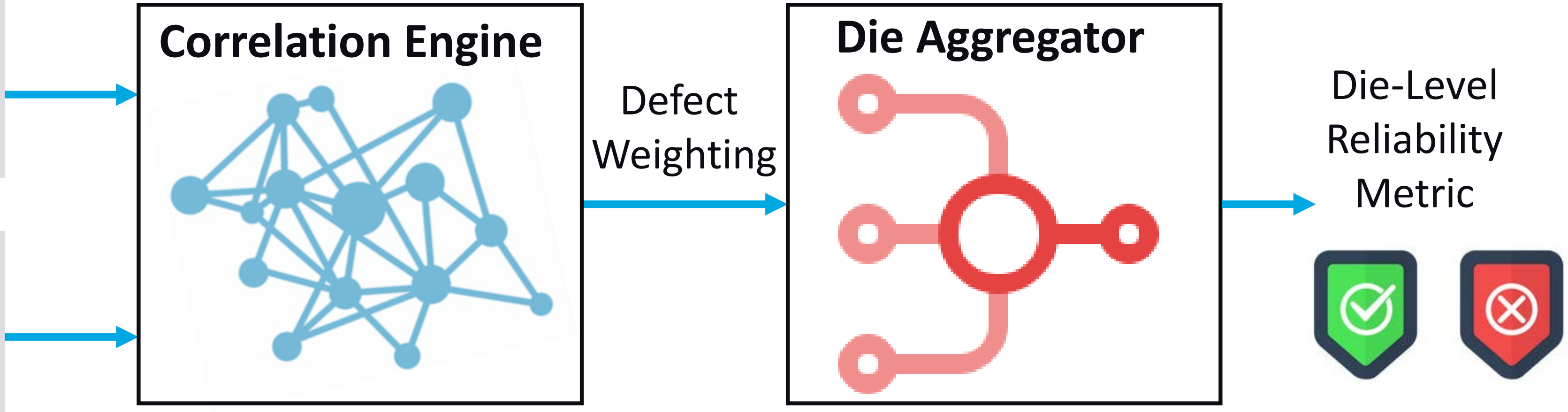
Uses advanced correlation engines to weight defect probability based on defect attributes

Latent Reliability Defect Data:

- SEM defect image review
- Electrical wafer sort
- Final test
- Burn-in
- Field returns
- Hit-back analysis

Inspection Defect Attributes:

- Defect type (rough bin)
- Defect size, shape, polarity, etc.
- Proximity to critical area
- In Die Region (e.g., test coverage gaps)
- Defect source analysis
- Modeled yield impact
- Spatial signature analysis
- Stacked layers and stacked die position



Correlation Engine

Defect Weighting

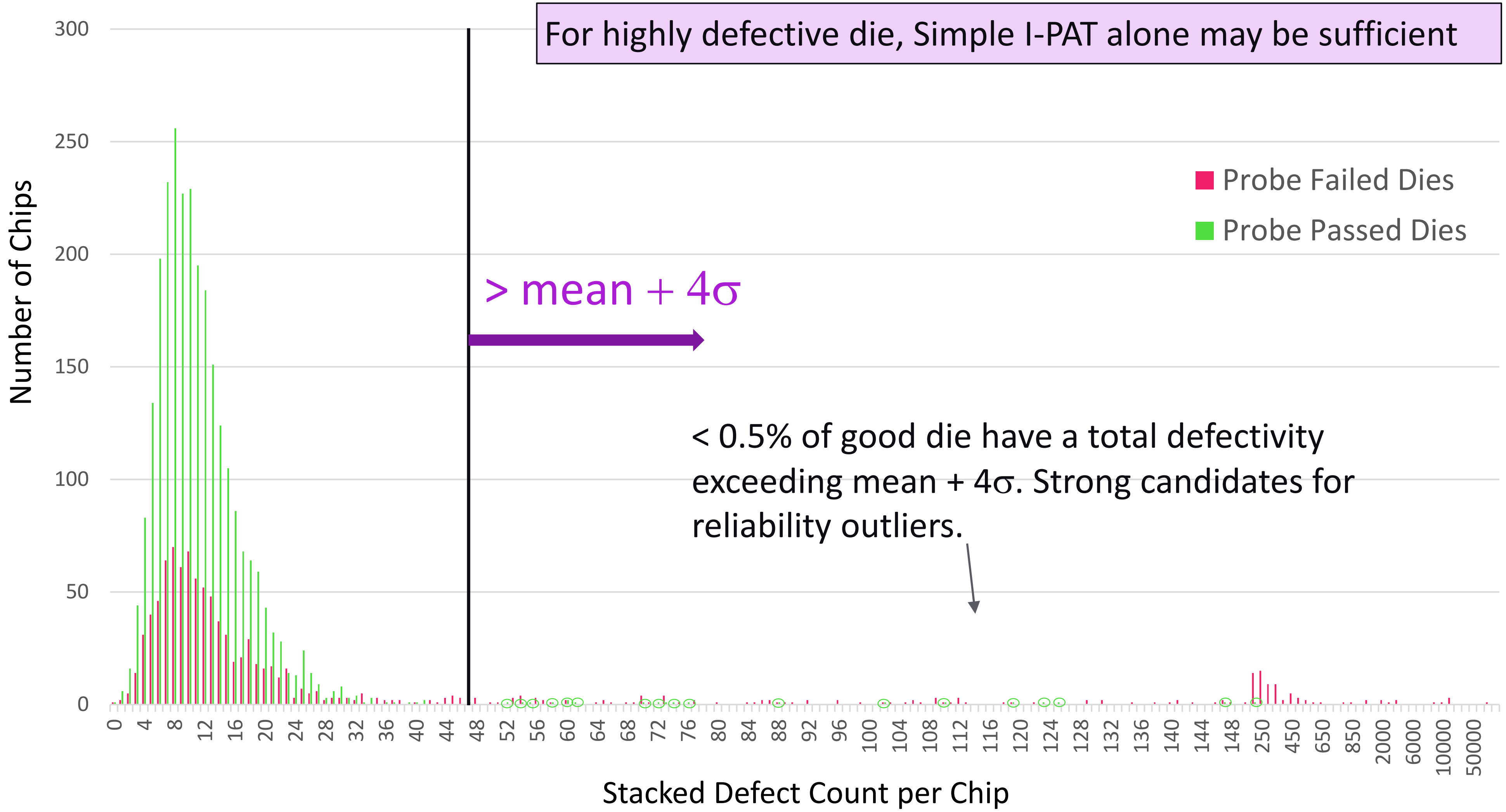
Die Aggregator

Die-Level Reliability Metric

Sample Results

28nm SOC device
~4000 die inspected at ~20 layers

1. Simple I-PAT (Defect Count Only)

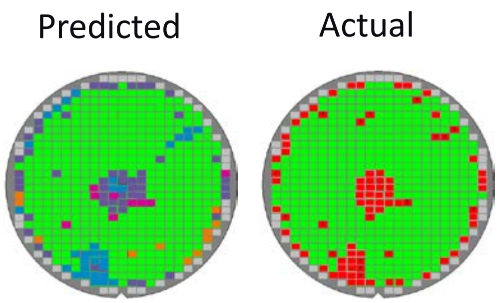


For highly defective die, Simple I-PAT alone may be sufficient

> mean + 4σ

< 0.5% of good die have a total defectivity exceeding mean + 4σ. Strong candidates for reliability outliers.

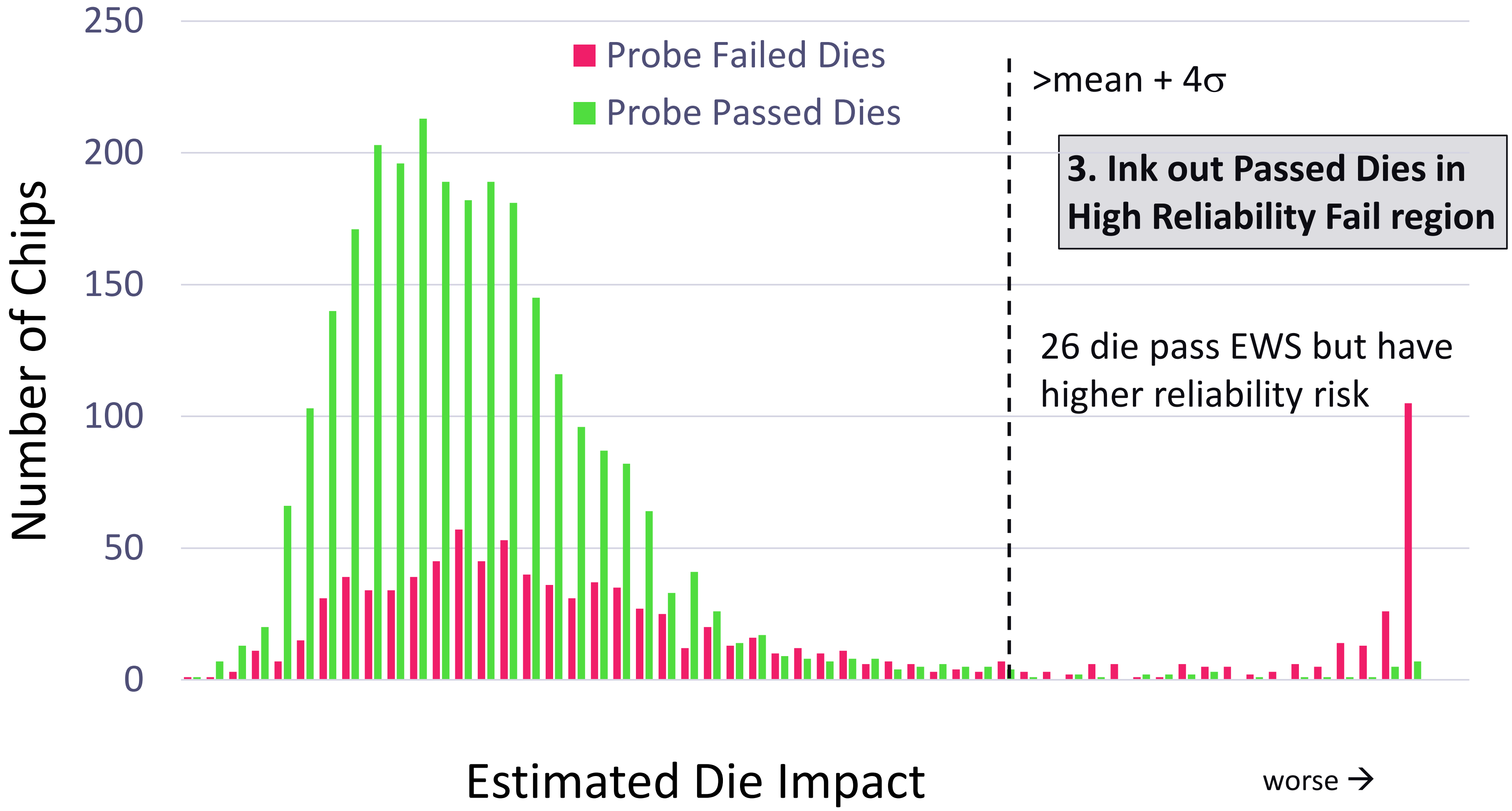
2. Smart I-PAT Using Defect Kill Probability (KPC)



Mockup for illustration only

1. Create a KPC Model to match Predicted Yield to Actual Yield*

2. Create a Histogram of Estimated Die Impact for the wafer



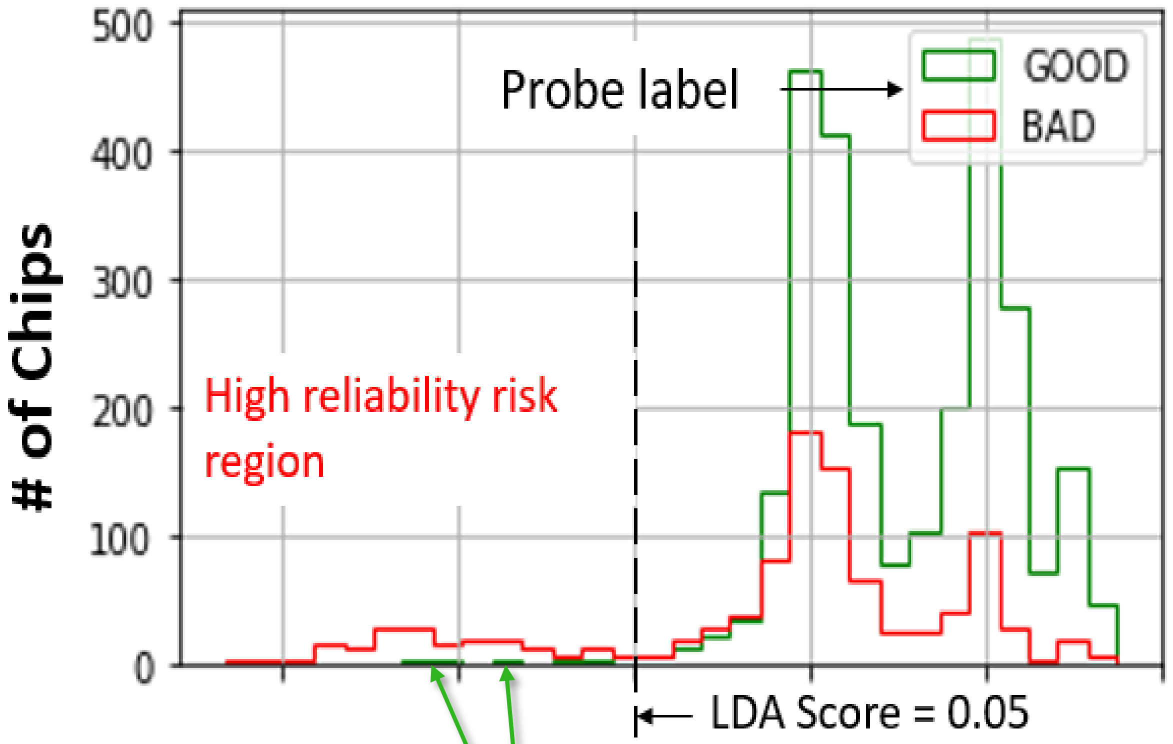
>mean + 4σ

3. Ink out Passed Dies in High Reliability Fail region

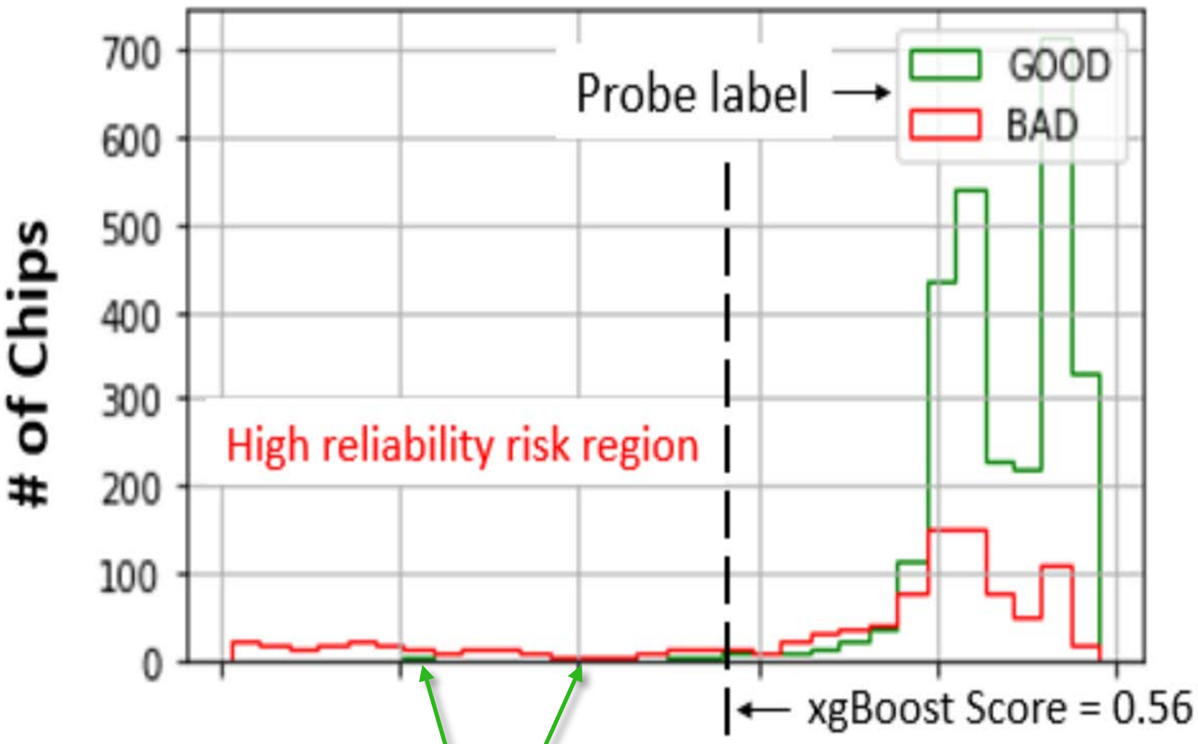
26 die pass EWS but have higher reliability risk

*defect limited yield

3. Smart I-PAT Using Defect Attributes and ML



Linear Discriminant Analysis (LDA)



xgBoost Model

Good Die in a Bad *Defect-Attribute* Neighborhood

Outlier Die Comparison Across Models

Six die that passed probe are flagged as outliers by 3+ models

Non-outlier die:

- *Reduce Burn-in?*
- *Reduce Test Coverage?*

	Die #	-14:20	-2:-3	-1:-1	7:27	-5:-29	7:-29	-9:-16	-5:24	-5:-6	7:-15	7:14	-22:4	-10:31	-26:20	-13:19	-1:0	7:32	14:32	27:-1	31:3	31:4	-25:20	7:-22	18:-26	22:20	-2:-2	-1:6	10:-27	36:-4
Simple I-PAT	12	X	X	X	X	X	X	X	X	X	X	X	X																	
Smart I-PAT: KPC	15	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X													
Smart I-PAT: ML-LDA	10	X	X	X	X										X			X	X	X	X	X								
Smart I-PAT: ML xgBoost	8	X				X								X	X								X	X	X	X				
Defect Guided G-PAT	7		X	X			X																				X	X	X	X

Ink Off

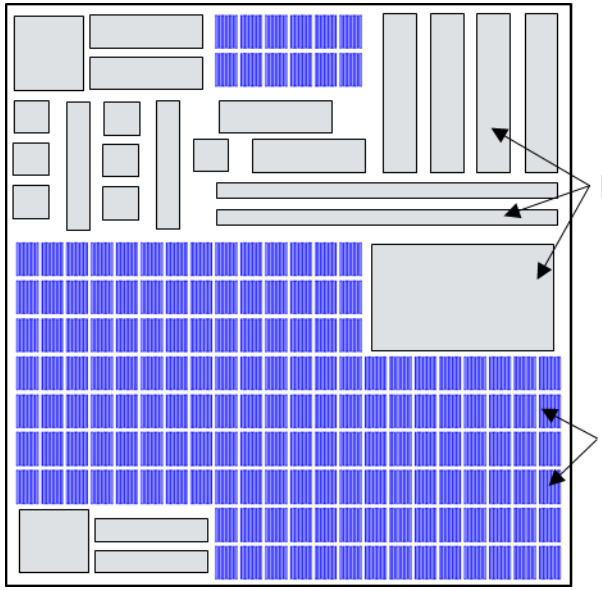
Send for Burn-in or Extended Test

The Usual Baseline

*Mean plus 4 sigma limit on all 5 algos

Next Steps: Smart I-PAT Based on In-Die Regions

In Die Region Layout



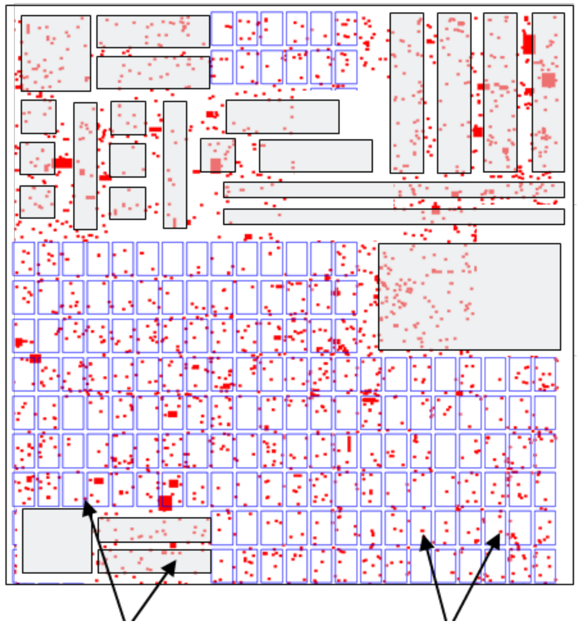
Non-Critical areas

Critical area

Different functional areas

- Different pattern densities
- Different sensitivity requirements
- Different yield impact

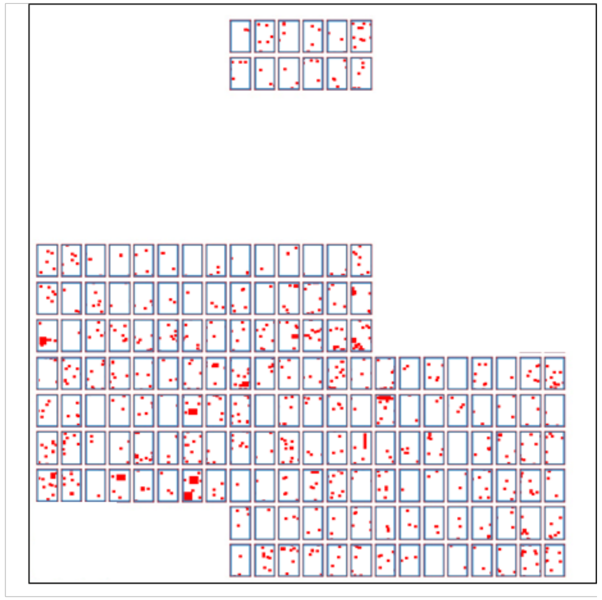
Stacked Die Map with all defects



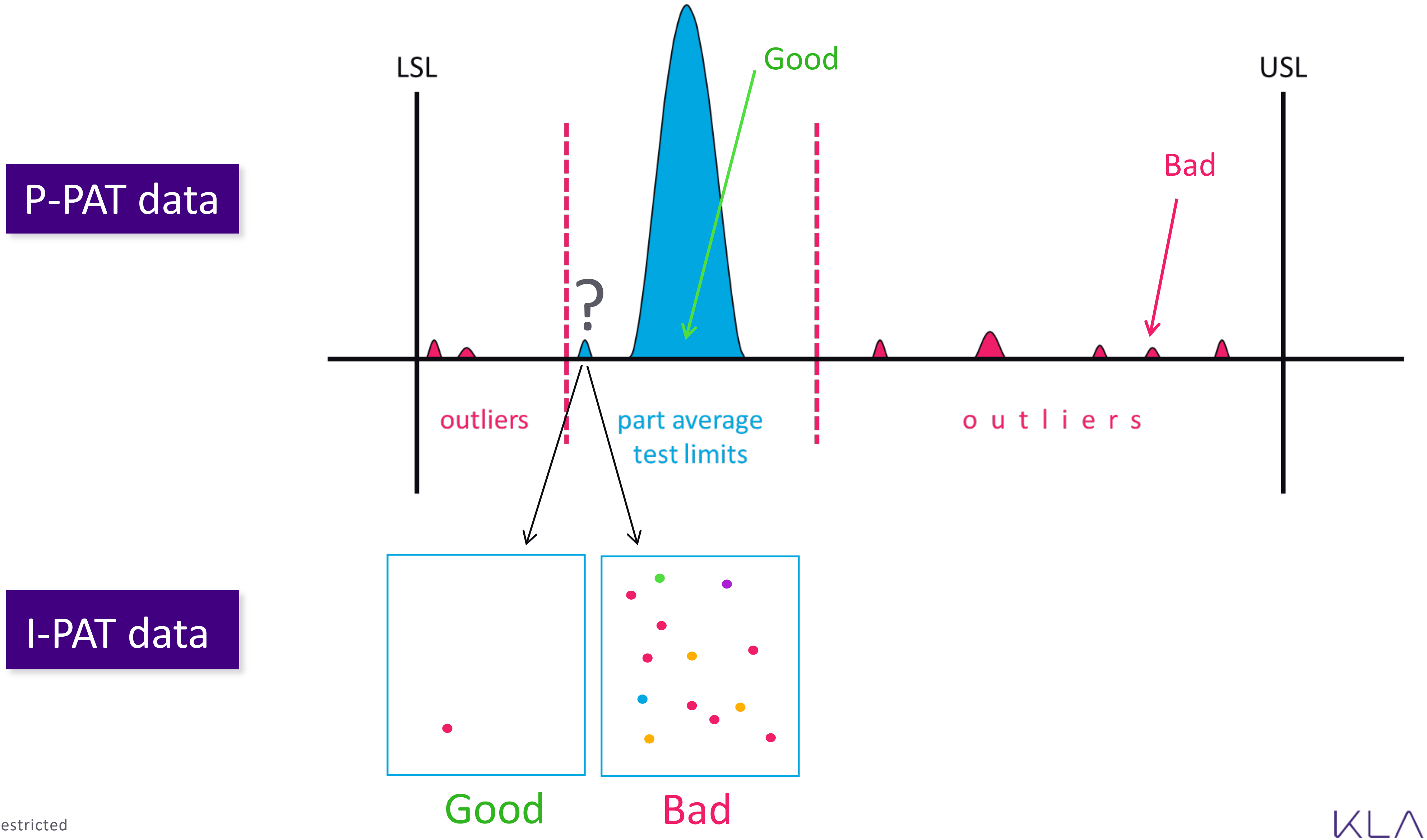
Embedded particle in open area

Embedded particle in dense pattern area

Stacked Die Map with only critical area defects

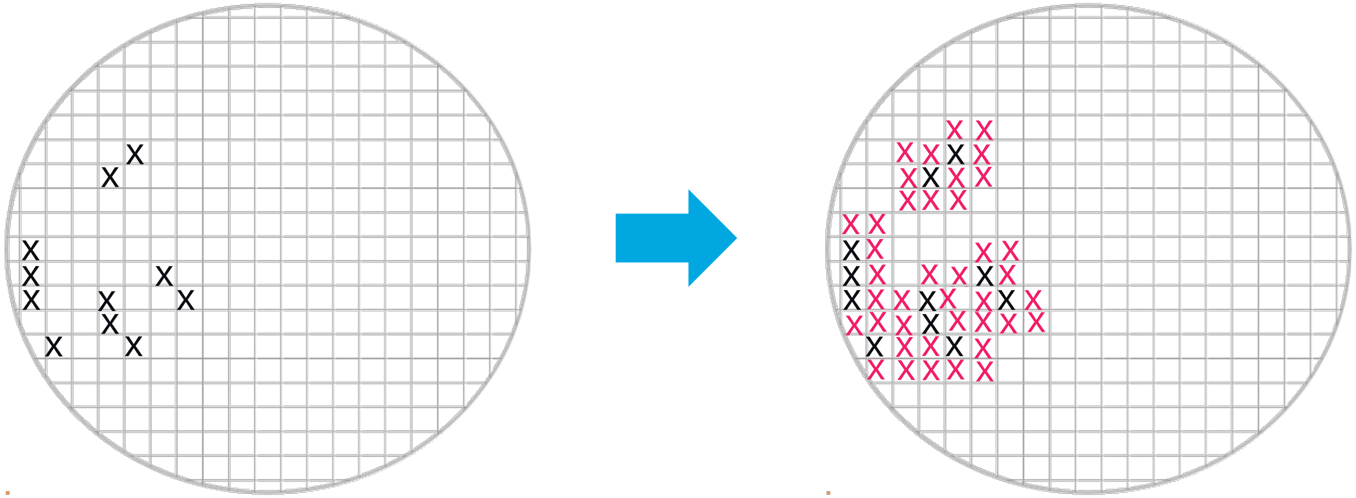


Next Steps: Feed Forward to Traditional P-PAT



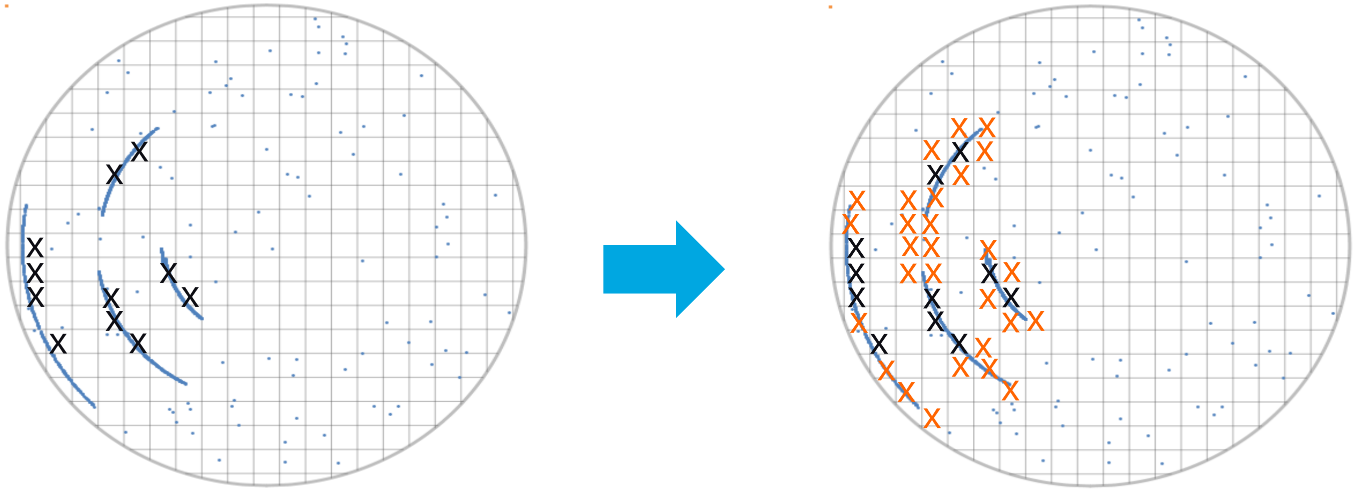
Next Steps: Feed Forward to Traditional G-PAT

Bad Die at Probe



Standalone G-PAT (GDBN) inks off neighboring die

Bad Die at Probe with Defect Signature Overlay shows bad die are actually part of a larger signature



I-PAT + G-PAT together can more precisely ink off potential outlier die that are part of the underlying signature

Summary

I-PAT may help the fab make smarter decisions, which may:

- Reduce reliability escapes
- Reduce overkill from P-PAT, G-PAT
- Reduce test costs
- Reduce burn-in costs, or
- Some combination of the above depending on how aggressively the threshold is set