

Process Watch: Monitoring for excursions in automotive fabs

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Author's Note: The Process Watch series explores key concepts about process control—defect inspection, metrology and data analytics—for the semiconductor industry. This article is the fourth in a series on process control strategies for automotive semiconductor devices.

The first three articles¹⁻³ in this series discussed methods that automotive semiconductor manufacturers can use to better meet the challenging quality requirements of their customers. The first paper addressed the impact of automotive IC reliability failures and the idea that combating them requires a "Zero Defect" mentality. The second paper discussed continuous improvement programs and strategies that automotive fabs implement to reduce the process defects that can become chip reliability problems. The third paper focused on the additional process control sensitivity requirements needed to capture potential latent (reliability) defects. This installment discusses excursion monitoring strategies across the entire automotive fab process so that non-conforming material can be quickly found and partitioned.

Semiconductor fabs that make automotive ICs typically offer automotive service packages (ASPs). These ASPs provide differentiated process flows – with elements such as more process control and process monitoring, or guaranteed use of golden process tools. The goal of ASPs is to help ensure that the chips produced meet the stringent reliability requirements of the automotive industry.

But even with the use of an automotive service package, excursions are inevitable, as they are with any controlled process. Recognizing this, automotive semiconductor fabs pay special attention to creating a comprehensive control plan for their critical process layers as part of their Process Failure Mode and Effects Analysis (PFMEA). The control plan details the process steps to be monitored and how they are monitored – specifying details such as the inspection sensitivity, sampling frequency and the exact process control systems to be used. A well-designed control plan will detect all excursions and keep "maverick" wafers from escaping the fab due to undersampling. Additionally, it will clearly indicate which

wafers are affected by each excursion so that they can be quarantined and more fully dispositioned – thereby ensuring that non-conforming devices will not inadvertently ship.

To meet these objectives, the control plan of an automotive service package will invariably require much more extensive inspection and metrology coverage than the control plan for production of ICs for consumer products. An analysis of process control benchmarking data from fabs running both automotive and non-automotive products at the same design rule have shown that the fabs implement more defect inspection steps and more types of process control (inspection and metrology) for the automotive products. The data reveals that on average:

- Automotive flows use approximately 1.5 to 2 times more defect inspection steps
- Automotive flows employ more frequent sampling, both as a percentage of lots and number of wafers per lot
- Automotive flows use additional sensitivity to capture the smaller defects that may affect reliability

The combined impact of these factors results in the typical automotive fab requiring 50% more process control capacity than their consumer product peers. A closer look reveals exactly how this capacity is deployed.

Figure 1 below shows an example of the number of lots between inspection points for both an automotive and a non-automotive process flow in the same fab. As a result of the increased number of inspection steps, if there is a defect excursion, it will be found much more quickly in the automotive flow. Finding the excursion sooner limits the lots at risk: a smaller and more clearly defined population of lots are exposed to the higher defect count, thereby helping serve the automotive traceability requirement. These excursion lots are then quarantined for high-sensitivity inspection of 100% of the wafers to disposition them for release, scrap, or when applicable, a downgrade to a non-automotive application.

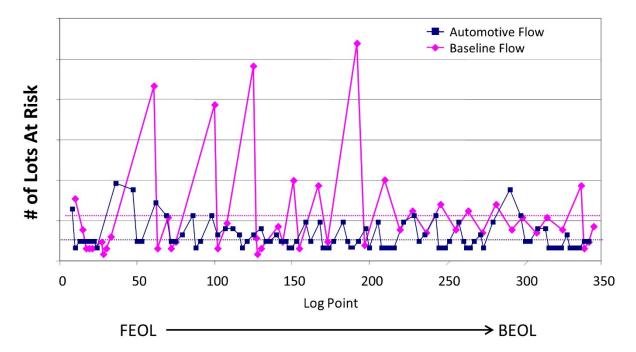


Figure 1. Example demonstrating the lots at risk between inspection points for an automotive process flow (blue) and a non-automotive (baseline) process blow (pink). The automotive process flow has many more inspection points in the FEOL and therefore fewer lots at risk when a defect excursion does occur.

The additional inspection points in the automotive service package have the added benefit of simplifying the search for the root cause of the excursion by reducing the range of potential sources. Fewer potential sources helps speed effective 8D investigations⁴ to find and fix the problem. Counterintuitively, the increased number of inspection points also tends to reduce production cycle time due to reduced variability in the line.⁵

While increasing inspection capacity helps monitor and contain process excursions, there remains risk to automotive IC quality. Because each wafer may take a unique path through the multitude of processing chambers available in the fab, the sum of minor variations and marginalities across hundreds of process steps can create "maverick" wafers. These wafers can easily slip through a control plan that relies heavily on sub-sampling, allowing at-risk die into the supply chain. To address this issue, many automotive fabs are adding high-speed macro defect inspection tools to their fleet to scan more wafers per lot. This significantly improves the probability of catching maverick wafers and preventing them from entering the automotive supply chain.

Newer generation macro defect inspection tools⁶ can combine the sensitivity and defect capture of many older generation brightfield and darkfield wafer defect inspection tools into a single platform that can operate at nearly 150 wafers per hour, keeping cost of ownership low. In larger design rule 200mm fabs,

the additional capacity often reveals multiple low-level excursions that had previously gone undetected, as shown in **Figure 2**.

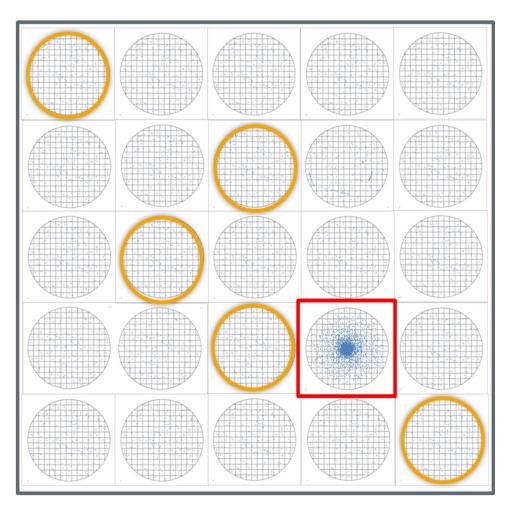


Figure 2. The legacy sample plan of 5 wafers per lot (yellow circles) would have allowed the single maverick wafer excursion (red square) to go undetected. High capacity macro defect inspection tools can stop escapes by reducing undersampling and the associated risks.

In advanced, smaller design rule fabs, macro defect inspection tools lack the needed sensitivity to replace the traditional line monitoring and patterned wafer excursion monitoring roles occupied by broadband plasma and laser scanning wafer defect inspection tools. However, their high capacity has found an important role in augmenting the existing sample plan to find wafer-level signatures that indicate a maverick wafer.

A recent development in automotive control strategies is the use of defect inspection for die-level screening. One such technique, known as Inline Defect Part Average Testing (I-PAT[™]), uses outlier

detection techniques to further enhance the fab's ability to recognize die that may pass electrical test but become reliability failures later due to latent defects. This method will be discussed in detail in the next installment of this series

About the Authors:

Dr. David W. Price and Jay Rathert are Senior Directors at KLA-Tencor Corp. Dr. Douglas Sutherland is a Principal Scientist at KLA-Tencor Corp. Over the last 15 years, they have worked directly with over 50 semiconductor IC manufacturers to help them optimize their overall process control strategy for a variety of specific markets, including implementation of strategies for automotive reliability, legacy fab cost and risk optimization, and advanced design rule time-to-market. The Process Watch series of articles attempts to summarize some of the universal lessons they have observed through these engagements.

References:

- 1. Price, Sutherland and Rathert, "Process Watch: The (Automotive) Problem With Semiconductors," *Solid State Technology*, January 2018.
- 2. Price, Sutherland and Rathert, "Process Watch: Baseline Yield Predicts Baseline Reliability," Solid State Technology, March 2018.
- 3. Price, Sutherland, Rathert, McCormack and Saville, "Process Watch: Automotive Defect Sensitivity Requirements," Solid State Technology, August 2018.
- 8D investigations involve a systematic approach to solving problems. https://en.wikipedia.org/wiki/Eight_disciplines_problem_solving
- 5. Sutherland and Price, "Process Watch: Process Control and Production Cycle Time," Solid State Technology, June 2016.
- 6. For example, see: https://www.kla-tencor.com/products/chip-manufacturing/defect-inspectionreview.html#product-8-series

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